PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference TJ0405-PCT	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. PCT/JP2004/015328	International filing date *(day/month/year)* 08.10.2004	Priority date *(day/month/year)* 20.10.2003

International Patent Classification (IPC) or national classification and IPC
H01L27/06, H01L27/088, H01L21/762, H01L21/8234

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1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 7 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 5 sheets, as follows:
      ☐ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☐ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☒	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
08.08.2005	25.01.2006

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/015328

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

   Description, Pages

   1-31 as originally filed

   Claims, Numbers

   1-14 as originally filed

   Drawings, Sheets

   1/16-16/16 as originally filed

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/JP2004/015328

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	4-14
	No:	Claims	1-3
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-14
Industrial applicability (IA)	Yes:	Claims	1-14
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VI Certain documents cited

1. Certain published documents (Rule 70.10)

and / or

2. Non-written disclosures (Rule 70.9)

see separate sheet

The following comments relate to items of the cover sheet where the corresponding cases have been crossed, as well as to eventual aspects concerning the form and content of the application and clarity of the claims.

1 Reference is made to the following documents:

D1: US 2002/043699 A1 (AKIYAMA HAJIME) 18 April 2002 (2002-04-18)
D2: GB-A-2 310 081 (INTERNATIONAL RECTIFIER CORPORATION) 13 August 1997 (1997-08-13)

2 The amendments filed with the letter of 05.08.2005 introduce subject-matter which extends beyond the disclosure of the international application as filed, contrary to Article 34(2)(b) PCT. The amendments concerned are the following:

2.1 In claim 1 (cf. lines 7-9) "a structure to separate ... " is now defined, which includes any type of structure, beyond the (at least one) trench filled with insulating material disclosed in the application as filed.

2.2 In claim 1 (cf. line 14) the wording "at least an output" appears to relate to a relay (NMOS and PMOS with their connection) as described in the description and figures but without its features, the non-inclusion of which in claim 1 results in an undue intermediate generalisation of its subject-matter.

2.3 In claim 4 (cf. lines 2-3), the newly introduced feature that "the high withstand voltage separating region surrounds ... regions" appears to be an undue generalisation of the features of claim 6 (one region (high or low voltage) surrounds the other and the withstand region is between and has a ring shape). Furthermore, the feature that the insulating partition is filled with insulating material in a trench has been removed, contrary to the requirements of Article 34(2)(b) PCT.

2.4 The removal from originally filed claims 12 and 13, on which present claims 12 and 13 are presently based, of the features " a plurality of fourth regions arranged in a ring shape ... first and second regions" results in an undue intermediate

generalisation of their subject-matter.

2.5 For the reasons explained above claims 1, 4, 12 and 13 are not admissible.

3 The present application does not comply with Article 33(2) PCT because the subject-matter of claims 1-3, insofar as they are admissible (cf. item 2 above), is not new.

3.1 The subject-matter of independent claim 1 is fully anticipated by the content of document D1 (cf. Figures 16-17 and associated text), which discloses semiconductor device having a high voltage region (HR), a low voltage region (connected to D1), a high withstand voltage region (region therebetween, e. g. 620, 630, 640) separating the high voltage region and the low voltage region, a relay (NR, PR) in the high withstand voltage region (620, 630, 640), an insulating partition (620, 630, 640) having a trench filled with insulating material (601) between the relay and one of the high voltage and low voltage regions, an output wiring (SL1, G1, D1) between the relay and the high voltage region or low voltage region bridging over the insulating partition.
It should be further noted that: first, the relay of D1 has a source and gate connection at one side, and a drain at another, as in the present application (see NMOS and PMOS) (Article 33(2) PCT); second, even if the relay circuit of the present application is specified in the claims (which is not at present), this would only be an obvious design alternative, which the skilled person would use in accordance with the type of desired high-low transition (Article 33(3) PCT).

3.2 The additional technical features of dependent claims 2-3 are also already known from the disclosure of document D1 (cf. Figures 16-17 and associated text).

4 The present application does not comply with Article 33(3) PCT because the subject-matter of claims 4-14, as long as the claims are admissible, does not involve an inventive step.

4.1 The subject-matter of present claim 4 differs from the disclosure of document D1 (cf.

figures 16-17 and associated text) in that the relay is arranged to form a ring shape which separates the high and low voltage regions. The objective problem to be solved derivable therefrom and solution thereto is, however, already known from document D2 (cf. page 3, lines 13-18; figures 3-15). Thus, it would be obvious to the skilled person to use the teaching of D2 and provide in a device as disclosed in D1 a relay being arranged to form a ring shape which separates the high and low voltage regions. Therefore, the subject-matter of present claim 4 does not involve an inventive step.

4.2 The additional technical features of claims 5-14 (the features of claims 6, 7, 12 and 13 considered as dependent from claim 4) are obvious choices or modifications readily available to the skilled person. Therefore, the subject-matter of claims 5-14 does not involve an inventive step.

4.3 The possible advantage of an apparatus defined by a claim having a combination of features of present claims 1, 4 and 6 (without substrate and conductivity types), duly amended to be admissible (cf. item 2 above), is at present not clear vis-à-vis the combined teaching of the cited prior art.

5 The following deficiencies should also be noted:

5.1 Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in documents D1-D2 is not mentioned in the description, nor are these documents identified therein.

5.2 Independent claim 1 is not in the two-part form in accordance with Rule 6.3(b) PCT, which in the present case would be appropriate, with those features known in combination from the prior art being placed in a preamble (Rule 6.3(b)(i) PCT) and with the remaining features being included in a characterising part (Rule 6.3(b)(ii) PCT).

5.3 The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

CLAIMS

1. (Amended) A semiconductor apparatus containing a low potential reference circuit region and a high potential reference circuit region between which signals are transmitted, the semiconductor apparatus comprising:

a high withstand voltage separating region arranged between the low and high potential reference circuit regions, the high withstand voltage separating region including a separating structure to separate both potential reference circuit regions;

a relay semiconductor device, formed in the high withstand voltage separating region, for transmitting a signal from one of the low and high potential reference circuit regions to the other of them; and

an insulating partition arranged between at least an output one of the low and high potential reference circuit regions and the relay semiconductor device, the insulating partition being filled with insulating material in a trench,

wherein output wiring of the relay semiconductor device is wired to an output one of the low and high potential reference circuit regions bridging over the insulating partition.

2. (Unchanged) A semiconductor apparatus according to claim 1 further comprising a substrate region arranged below the low and high potential reference circuit regions, wherein

bottom portion of the insulating partition extends to the substrate region, and

the insulation partition surrounds the relay semiconductor device.

3. (Unchanged) A semiconductor apparatus according to claim 1 or claim 2 further comprising a group of insulating partitions arranged between the low and high potential reference circuit regions, the group of insulating partitions dividing space between the low and high potential reference circuit regions into plural regions.

4. (Amended) A semiconductor apparatus according to claim 1,

wherein the high withstand voltage separating region surrounds one of the low and high potential reference circuit regions,

a plurality of the relay semiconductor devices are arranged to form a ring shape in the high withstand voltage separating region,

each relay semiconductor device is surrounded with an insulating partition, and

output wiring of each relay semiconductor device is wired to an output one of the low and high potential reference circuit regions bridging over the insulating partition.

5. (Unchanged) A semiconductor apparatus according to claim 1 or claim 4 further comprising:

a substrate region arranged below the low and high potential reference circuit regions; and

an insulating layer embedded between the low and high potential reference circuit regions and the substrate region, the insulating layer electrically insulating the low and high potential reference circuit regions from the substrate region,

wherein bottom portions of the insulating partitions extend to the insulating layer and the insulation partitions surround the relay semiconductor devices.

6. (Amended) A semiconductor apparatus according to claim 1 comprising:

a semiconductor substrate of first conduction type;

wherein the low and high potential reference circuit regions are regions of second conduction type formed on a main surface of the semiconductor substrate so that one of the regions surrounds the other in separated relation, and

the high withstand voltage separating region is a region formed in a ring shape between the low and high potential reference circuit regions.

7. (Amended) A semiconductor apparatus according to claim 1 comprising:

a semiconductor substrate of either first or second conduction type; and

an insulating film formed on the semiconductor substrate;

wherein the low and high potential reference circuit regions are regions of second conduction type formed on the insulating film so that one of the regions surrounds the other in separated relation, and

the high withstand voltage separating region is a region formed in a ring shape between the low and high potential reference circuit regions.

8. (Unchanged) A semiconductor apparatus according to claim 6 or claim 7, wherein

bottom portion of the insulating partition extends to either the semiconductor substrate or the insulating film, and

the insulating partition surrounds periphery of a relay

13. A semiconductor apparatus according to claim 1 comprising:

a semiconductor substrate of either first or second conduction type; and

an insulating film formed on the semiconductor substrate;

wherein the low and high potential reference circuit regions are regions of second conduction type formed on the insulating film so that one of the regions surrounds the other in separated relation.

14. (Unchanged) A semiconductor apparatus according to claim 12 or claim 13, wherein

bottom portion of the insulating partition extends to either the semiconductor substrate or the insulating film, and

the insulating partition surrounds periphery of a relay semiconductor device in a fourth region from at least three directions.